AMENDMENTS TO THE CLAIMS

1. **(Canceled)**

2. **(Currently Amended)** A method according to claim [[1]] 17, wherein said processing step is performed in a state in which said semiconductor substrate is grounded.

3-12. **(Canceled)**

13. **(Currently Amended)** A method according to claim [[1]] 17, further comprising:

forming on said substrate a second N region that is independent of said first N region.

14. **(Previously Presented)** A method according to claim 13, wherein the total surface area of said first N region and said second N region is 100 to 1/100 times the total surface area of said P region.

15. **(Previously Presented)** A method according to claim 13, wherein said second N region is formed at the periphery of said substrate.

16. **(Previously Presented)** A method according to claim 13, wherein said wiring contains any one of Cu, Al and W as its main component.

17. **(Previously Presented)** A method for manufacturing a semiconductor device comprising:

forming a first N region and a P region on a substrate, forming wiring so as to connect one or both of the first N and the P regions; and

performing a processing step on a semiconductor substrate on which the upper surface of said wiring is exposed using a liquid applied to said semiconductor substrate and a light source radiating light onto said semiconductor substrate,

wherein said processing step is performed in a state in which the wavelength of light radiated onto said semiconductor substrate is 500 nm to less than 1 μm,

wherein said processing step is a cleaning step performed during, before or after a step that includes chemical mechanical polishing (CMP) for forming said wiring, said wavelength of light radiated onto said semiconductor substrate being 500 nm to less than 1 μm in order to reduce an electromotive force at a PN junction in said semiconductor substrate, thereby inhibiting galvanic effects due to photoexcitation before, during or after said step including CMP, and preventing oxidation of a surface of said wiring,

wherein the exposing of the upper surface of said wiring of the semiconductor substrate to the liquid is performed concurrently with the exposing of the upper surface of said semiconductor substrate to the light source radiating light.

18. **(Currently Amended)** A method for manufacturing a semiconductor device comprising:

forming a first N region and a P region on a semiconductor substrate;

forming wiring so as to connect at least one of the P region and the N region; and

exposing the upper surface of said wiring using a liquid applied to said semiconductor substrate and a light source radiating light onto said semiconductor substrate;

wherein said ~~processing~~ exposing step is a cleaning step performed during, before or after a step that includes chemical mechanical polishing (CMP) for forming said wiring; and

wherein said ~~processing~~ exposing step is performed in a state in which the wavelength of light radiated onto said semiconductor substrate is 500 nm to less than 1 μm in order to reduce an electromotive force at a PN junction in said semiconductor substrate, thereby inhibiting galvanic effects due to photoexcitation before, during or after said step including CMP, and preventing oxidation of a surface of said wiring.

19. (New) A method according to claim 18, wherein said exposing step is performed in a state in which said semiconductor substrate is grounded.

20. (New) A method according to claim 18, further comprising:

forming on said substrate a second N region that is independent of said first N region.

21. (New) A method according to claim 20, wherein the total surface area of said first N region and said second N region is 100 to 1/100 times the total surface area of said P region.

22. **(New)** A method according to claim 20, wherein said second N region is formed at the periphery of said substrate.

23. **(New)** A method according to claim 20, wherein said wiring contains any one of Cu, Al and W as its main component.